What is claimed is:

1. An apparatus for selecting test patterns comprising:

a first test pattern selecting module configured to classify a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

a fault simulation module configured to simulate whether the plurality of selected test patterns and the plurality of unselected test patterns detect a plurality of faults estimated to occur in the logic circuit;

a weighting module configured to add weight reflecting a plurality of layout elements of the logic circuit to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and define the plurality of first undetected faults that are given the weight as a plurality of first weighted undetected faults;

a fault sampling module configured to extract a plurality of second undetected faults from the plurality of first weighted undetected faults; and

a second test pattern selecting module configured to extract a plurality of additionally selected test patterns that detects complementarily the plurality

of second undetected faults from each other from the plurality of unselected test patterns based on a criterion of the added weight.

2. The apparatus of claim 1, wherein the second test pattern selecting module further comprising:

a candidate test pattern selecting module configured to select a plurality of candidate test patterns that detect the plurality of second undetected faults from the plurality of unselected test patterns based on a first criterion of an evaluation value reflecting the added weight among the plurality of second undetected faults of detected faults by each of the plurality of unselected test patterns and a pattern length of each of the plurality of the unselected test patterns; and

an additionally selected test pattern selecting module configured to exclude from processing the plurality of candidate test patterns failing to fulfill a second criterion of the evaluation value and select an additionally selected test pattern by which the evaluation value is a maximum from the plurality of candidate test patterns and exclude from processing among the plurality of second undetected faults detected faults by the additionally selected test pattern and update the evaluation value.

3. A computer implemented method for selecting test patterns comprising:

classifying a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion;

simulating whether the plurality of selected test patterns detects a plurality of faults estimated to occur in the logic circuit;

adding a weight reflecting a plurality of layout elements of the logic circuit to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and defining the plurality of first undetected faults that are added the weights as a plurality of first weighted undetected faults;

extracting a plurality of second undetected faults from the plurality of first weighted undetected faults based on an extracting condition;

simulating whether the plurality of unselected test patterns detects the plurality of second undetected faults; and

selecting a plurality of additionally selected test patterns that detects complementarily the plurality

of second undetected faults from each other from the plurality of unselected test patterns based on a criterion of the added weight.

4. The computer implemented method of claim 3, wherein the reliability criterion is a functional verification coverage.

5. The computer implemented method of claim 3, wherein the reliability criterion is a coverage of the plurality of faults.

6. The computer implemented method of claim 3, wherein the extracting condition is a random sampling.

7. The computer implemented method of claim 3, wherein the extracting condition is value proportional to the added weight.

8. The computer implemented method of claim 3, wherein the selecting a plurality of additionally selected test patterns further comprising:

selecting a plurality of candidate test patterns that detect the plurality of second undetected faults from the plurality of unselected test patterns based

on a first criterion of an evaluation value reflecting the added weight among the plurality of second undetected faults of detected faults by each of the plurality of unselected test patterns and a pattern length of each of the plurality of the unselected test patterns;

excluding from processing the plurality of candidate test patterns failing to fulfill a second criterion of the evaluation value;

extracting an additionally selected test pattern by which the evaluation value is a maximum from the plurality of candidate test patterns; and

excluding from processing among the plurality of second undetected faults detected faults by the additional selected test pattern and updating the evaluation value.

9. A computer program product for controlling a computer system so as to select test patterns, the computer program product comprising:

instructions configured to classify a plurality of verification patterns of a logic circuit of an LSI into a plurality of selected test patterns fulfilling a reliability criterion and a plurality of unselected test patterns failing to fulfill the reliability criterion within the computer system;

instructions configured to simulate whether the plurality of selected test patterns detects a plurality of faults estimated to occur in the logic circuit within the computer system;

instructions configured to add a weight reflecting a plurality of layout elements of the logic circuit to each of a plurality of first undetected faults that are undetected by the plurality of selected test patterns and define the plurality of first undetected faults that are added the weights as a plurality of first weighted undetected faults within the computer system;

instructions configured to extract a plurality of second undetected faults from the plurality of first weighted undetected faults based on an extracting condition within the computer system;

instructions configured to simulate whether the plurality of unselected test patterns detects the plurality of second undetected faults within the computer system; and

instructions configured to select a plurality of additionally selected test patterns that detects complementarily the plurality of second undetected faults from each other from the plurality of unselected test patterns based on a criterion of the added weight within the computer system.

10. The computer program product of claim 9, wherein the reliability criterion is a functional verification coverage.

11. The computer program product of claim 9, wherein the reliability criterion is a coverage of the plurality of faults.

12. The computer program product of claim 9, wherein the extracting condition is a random sampling.

13. The computer program product of claim 9, wherein the extracting condition is value proportional to the added weight.

14. The computer program product of claim 9, wherein the second extracting instructions further comprising:

instructions configured to extract a plurality of candidate test patterns that detect the plurality of second undetected faults from the plurality of unselected test patterns based on a first criterion of an evaluation value reflecting the added weight among the plurality of second undetected faults of detected faults by each of the plurality of unselected

test patterns and a pattern length of each of the plurality of the unselected test patterns within the computer system;

instructions configured to exclude from processing the plurality of candidate test patterns failing to fulfill a second criterion of the evaluation value within the computer system;

instructions configured to select an additionally selected test pattern by which the evaluation value is a maximum from the plurality of candidate test patterns within the computer system; and

instructions configured to exclude from processing among the plurality of second undetected faults detected faults by the additional selected test pattern and update the evaluation value within the computer system.